AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Cancelled)

2. (Currently Amended) The component of claim 5 or 6 [[1]], wherein the electrically conductive connections comprise bumps.

3 and 4. (Cancelled)

5. (Currently Amended) A component comprising:

a chip having a top surface and having a bottom surface that includes electrically conductive structures;

a carrier substrate having a top surface that includes connecting areas, the chip being mounted in a flip chip arrangement on the carrier substrate via electrically conductive connections between the electrically conductive structures and the connecting areas;

a support element at the top surface of the carrier substrate, the support element surrounding the chip but not touching the chip; and

a seal that borders the chip and the support element;

wherein the support element supports the seal;

wherein the support element and the seal are configured to reduce an affect of mechanical forces on the electrically conductive connections that results from temperature variations;

~~The component of claim 1,~~ wherein the seal comprises[[:]] a composite comprising a dielectric layer and a metal layer, the composite forming a seal to the carrier substrate outside of an area that corresponds to the chip; and

wherein the chip has a thickness such that a force resulting from thermal expansion of an electrically conductive connection in a temperature range between -60° C and 85° C is a maximum of 2 Newtons.

6. (Currently Amended) A component comprising:

a chip having a top surface and having a bottom surface that includes electrically conductive structures;

a carrier substrate having a top surface that includes connecting areas, the chip being mounted in a flip chip arrangement on the carrier substrate via electrically conductive connections between the electrically conductive structures and the connecting areas;

a support element at the top surface of the carrier substrate, the support element surrounding the chip but not touching the chip; and

a seal that borders the chip and the support element;

wherein the support element supports the seal;

wherein the support element and the seal are configured to reduce an affect of mechanical forces on the electrically conductive connections that results from temperature variations;

~~The component of claim 1,~~ wherein the seal comprises[[:]] a composite comprising a dielectric layer and a metal layer above the dielectric layer relative to the top surface of the chip, the composite forming a seal to the carrier substrate outside of an area that corresponds to the chip; and

wherein the dielectric layer has a modulus of elasticity of less than 1 Gpa, a thickness of less than 20 μm, or a coefficient of thermal expansion that is greater than $\alpha_{bump}/2$ and that is less than 2 α_{bump}, where α_{bump} is a coefficient of thermal expansion for at least one of the electrically conductive connections.

7. (Currently Amended) The component of claim 5 or 6 ~~1~~, wherein the support element comprises a shrink frame that substantially encloses the chip.

8. (Currently Amended) The component of claim 7~~, further comprising a metal layer that substantially covers the top surface of the chip~~; wherein the shrink frame forms a seal to the carrier substrate.

9. (Currently Amended) The component of claim 5 or 6 ~~1, 5, 6, or 7~~, wherein the chip has side surfaces that are sloped so that a cross-section of the chip tapers toward the carrier substrate.

10. (Currently Amended) The component of claim 5 or 6 ~~1, 5, 6, or 7~~, wherein the chip has side surfaces that comprise at least one step.

11. (Currently Amended) The component of claim 5 or 6 [[1]], wherein the seal covers edge areas of the chip and the support element; and

wherein the seal does not cover the top surface of the chip.

12. (Currently Amended) The component of claim 5 or 6 [[1]], ~~further comprising~~ a wherein the metal layer is over ~~above the seal relative to the top surface of the chip, the metal layer being on~~ edge areas of the support element and/or on edge areas of the carrier substrate.

13. (Currently Amended) The component of claim 5 or 6 [[3]], wherein the dielectric layer completely covers the chip and the support element, the dielectric layer forming a seal to the carrier substrate only in areas that do not correspond to the support element so that the chip and the support element are in a shared space that is formed between the dielectric layer and the top surface of the carrier substrate.

14. (Currently Amended) The component of claim 5 or 6 [[3]], wherein the dielectric layer completely covers the top surface of the chip and seals to the support element, the support element comprising a hermetically tight material.

15. (Cancelled)

16. (Currently Amended) The component of claim 5 or 6 [[3]], further comprising a filling compound on the dielectric layer.

17. (Currently Amended) The component of claim 16, ~~further comprising a~~ wherein the metal layer ~~that forms a seal with the support element outside of an area that corresponds to the chip, or that~~ forms a seal ~~with~~ to the carrier substrate outside of an area that corresponds to the support element.

18. (Currently Amended) The component of claim 5 or 6 ~~1 or 7~~, further comprising a contact metallization on side surfaces of the chip that face the carrier substrate;

wherein the support element comprises a solder frame, the support element being soldered to a contact metallization of the chip.

19. (Currently Amended) The component of claim 5 or 6 ~~18~~, further comprising a metal layer ~~above~~ on a top surface of the chip.

20 and 21. (Cancelled)

22. (Currently Amended) The component of claim 5 or 6 [[3]], wherein the dielectric layer comprises at least one of a plastic, an organic plastic, a laminate film, a glass solder and a resin.

23. (Currently Amended) The component of claim 5 or 6 [[1]], wherein the support element comprises at least one of metal, a ceramic material and plastic.

24. (Currently Amended) The component of claim 5 or 6 [[1]], wherein the support element corresponds to a boundary of an indentation on the carrier substrate.

25. (Currently Amended) The component of claim 5 or 6 [[1]], wherein a height of the support element does not exceed a distance between the top surface of the carrier substrate and a bottom edge of the chip; and

wherein an the inner edge of the support element is under the bottom edge of the chip.

26. (Currently Amended) The component of claim 5 or 6 [[1]], wherein a height of the support element corresponds to, or exceeds, a distance between the top surface of the carrier substrate and a bottom edge of the chip.

27. (Currently Amended) The component of claim 5 or 6 ~~1, 5, 6, or 7~~, wherein the carrier substrate comprises a low temperature cofired ceramic.

28. (Currently Amended) The component of claim 5 or 6 ~~1, 5, 6, or 7~~, further comprising surface-mounted-device-capable external contacts on a bottom surface of the carrier substrate.

29. (Currently Amended) The component of claim 5 or 6 ~~1, 5, 6, or 7~~, wherein the carrier substrate comprises at least two dielectric layers.

30. (Currently Amended) The component of claim 5 or 6 ~~1, 5, 6, or 7~~, wherein the chip comprises at least one surface acoustic wave resonator or at least one bulk acoustic wave resonator ~~that works with acoustic surface waves or acoustic volume waves~~.

31. (Previously Presented) The component of claim 5 or 6 ~~1, 5, 6, or 7~~, further comprising ~~similar or different~~ one or more additional chips that are attached to the carrier substrate and that are ~~similarly~~ encapsulated using at least one support element and seal.

32 to 39. (Cancelled)